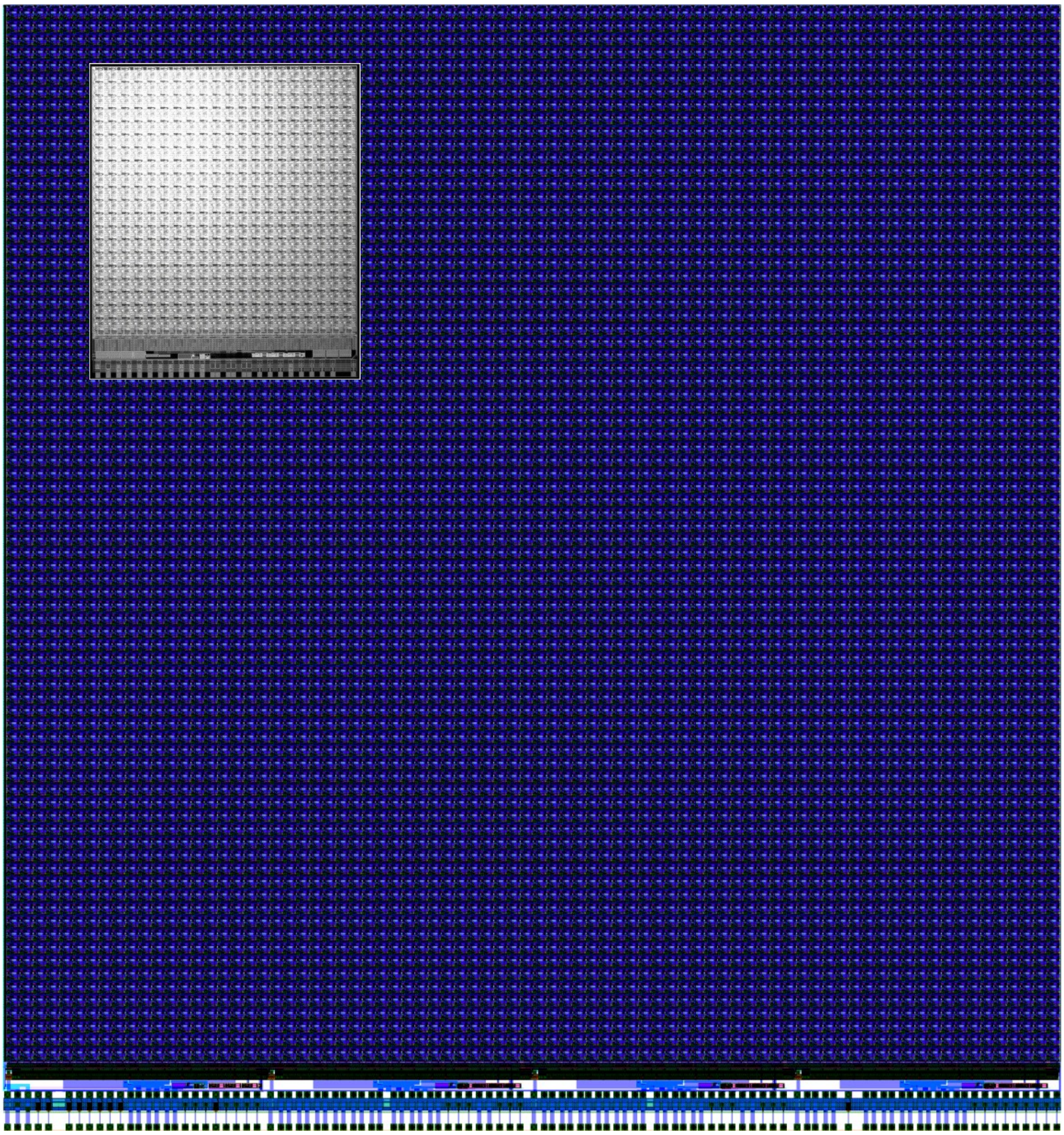
HEXITEC ASIC 20x20 and 80x80 User Manual



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1. Introduction

The HEXITEC ASICs were developed to provide a new range of detectors for high energy X-ray imaging. The HEXITEC ASICs are designed to measure the energy and position of all X-ray photons that are detected by the Cd(Zn)Te semiconductor material that is bump bonded to the ASIC. The HEXITEC ASICs have been designed to measure the energy of every photon with the best energy resolution possible and to continually sequentially output all measurements on all pixels. The energy resolution is achieved by having minimal high frequency clocks operating during data collection and tolerating the leakage current from the Cd(Zn)Te detectors. Bump bonding the Cd(Zn)Te material provides a low capacitance input to the ASIC (300fF/pixel estimated) to aid the low noise performance of the ASICs. The ASICs have an array of 20x20 or 80x80 readout pixels on a pitch of 250μm x 250μm. The small pixels give good imaging performance and make use of the small pixel effect to negate the poor hole transport in Cd(Zn)Te. The ASICs have been designed and manufactured on a standard 0.35μm process.

2. Specifications

2.1 Functional

20x20 and 80x80 pixellated readout ASIC for CdZnTe
250μm x 250μm pixel size
2μs Peaking Time
Peak Hold
Primary High Gain Range 250e- to 40ke- (20x20 and 80x80)
Secondary Low Gain Range 2ke- to 400ke- (20x20) or 1ke- to 133ke- (80x80)
Spectral resolution 20e- rms at 1ke-
Detector leakage immunity up to 250pA
Rolling shutter architecture read-out
Windowed readout, calibration and power down

2.2 Physical

Process: 0.35μm standard N-well CMOS
Size: 5.1x6mm^2 (20x20) and 20.25x21.53mm^2 (80x80); both are 0.72mm thick.
Pad size: 95 x 95 μm^2 (wire bonding), 52 x 52 μm^2 (gold stud bonding)
Analogue input gold stud bonding pads: 250 μm pitch, 20x20 and 80x80 array
I/O bonding and power/bias pads: variable pitch on 100μm grid, on one edge of the ASIC

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3. Functional Description

3.1 Summary

The HEXITEC ASIC consists of 20x20 or 80x80 pixels on a pitch of 250μm. Each pixel contains a 52μm bond pad which can be gold stud-bonded to a CZT detector. Figure 1 shows a block diagram of the electronics contained in each HEXITEC ASIC pixel. Charge is read out from each of the CZT detector pixels using a charge amplifier, which has a selectable range, and a feedback circuit which compensates for detector leakage currents optimised for <250pA but can operate at higher leakages.

The output from the each charge amplifier is filtered by a 2μs peaking circuit comprising a CR-RC shaper followed by a 2nd order low-pass filter. A peak hold circuit maintains the voltage at the peak of the shaped signal until it can be read-out.

Three track-and-hold buffers are used to sample the shaper and peak-hold voltages sequentially prior to the pixel being read out. When read-out occurs, the output from the pixel comprises the two samples from the shaper output and the one sample of the peak hold output. These three signals are used to veto incorrect peak hold data due to partly developed signals or incorrect peak hold reset levels. Switches are enabled which connect one pixel in each column of the pixel array to shared column outputs.

A calibration circuit is included for characterising the pixel electronics.

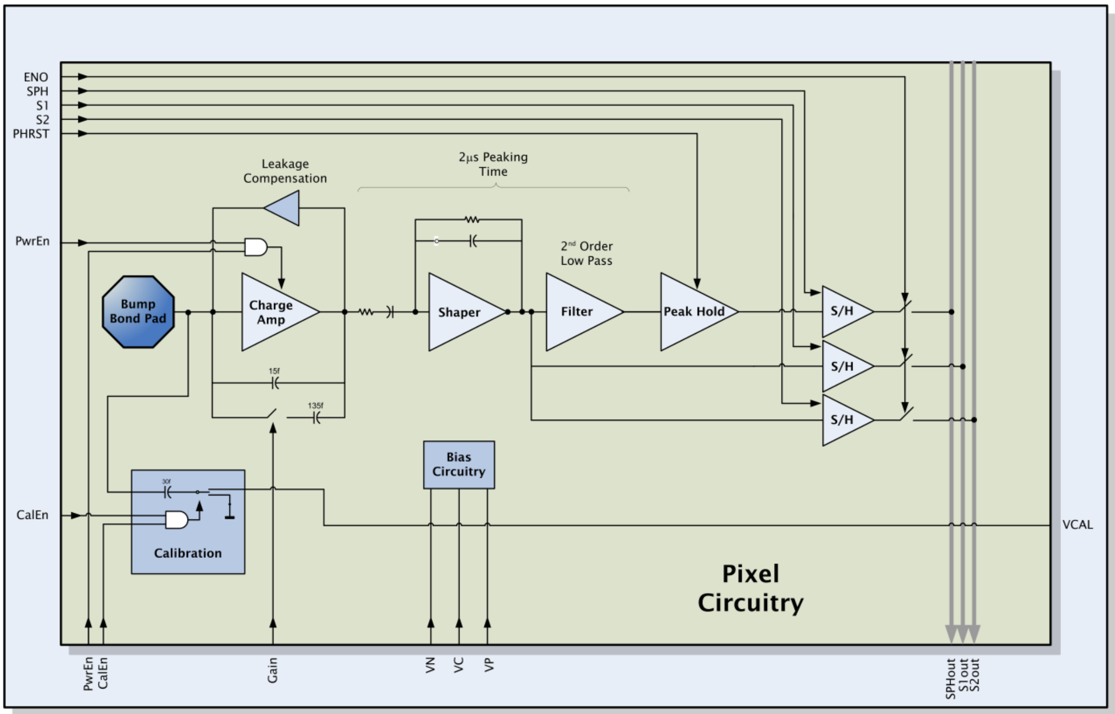

Figure 1. Block diagram of the Pixel in the 20x20 ASIC. The 80x80 is identical apart from a 35fF feedback capacitor in place of the 135fF.

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Read-out logic controls the sequencing of data from the HEXTIEC ASIC pixel array. Figure 2 shows a block diagram of the top level of the ASIC for the 20x20 pixel example. The 80x80 ASIC is controlled in the same manner with the loading of data repeated but with 80bit long registers and the readout conducted by 4 parallel outputs for 4 blocks of 80 rows and 20 columns.

Three programmable registers, 20bit or 80bit, can be used to define regions of interest within the pixel array. The first register defines the regions that will be read out, the second defines regions which will be powered down, and the third defines regions where the calibrate circuit is enabled.

The HEXITEC ASIC pixel array is read out using a rolling shutter technique. A row select register is used to select the row which is to be read out. The data from each pixel becomes available on all column outputs at the same time, and at this point the peak hold circuits in that row can be reset to accept new data. The data being held on the column output is read out through a column multiplexer. The column readout rate is up to 25MHz, typically 20MHz, and the total frame rate depends on the number of pixels being read out.

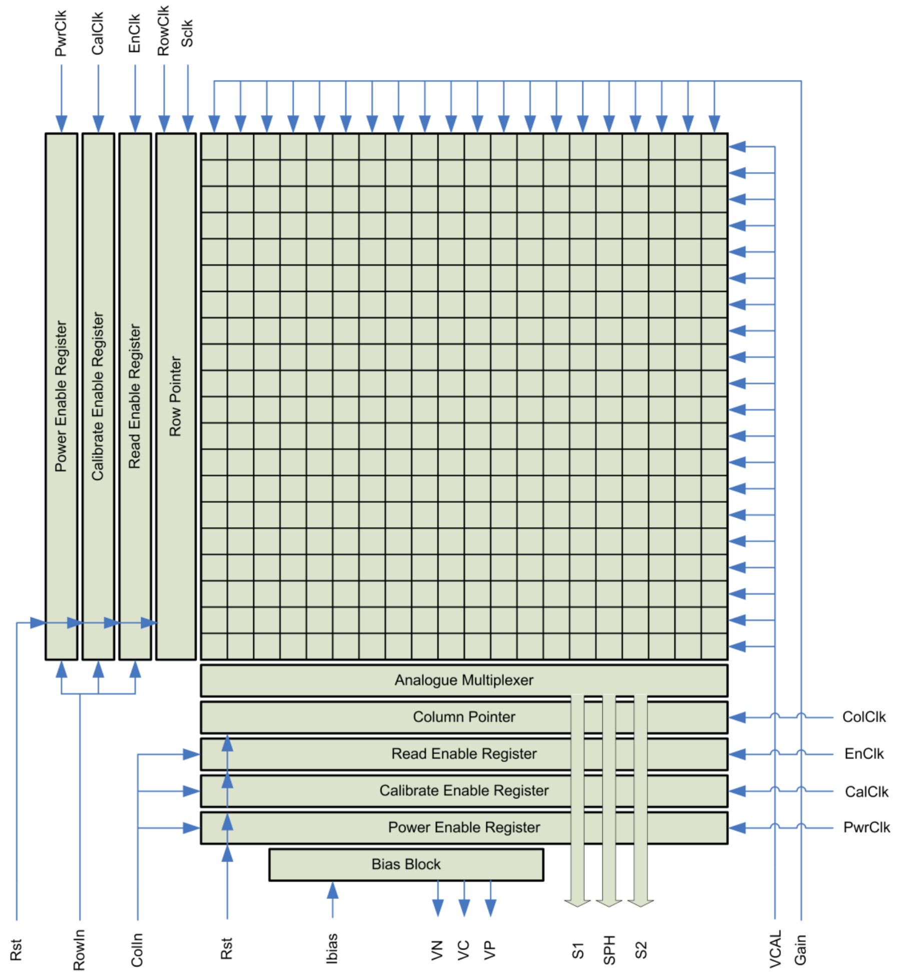

Figure 2. Block diagram of the HEXITEC ASIC

3.2 Preamplifier

The preamplifier takes the charge generated within the detector and integrates it onto a feedback capacitor. The charge to voltage gain is inversely proportional to the size of the feedback capacitor of which there are two sizes available. This allows the selection of two different input ranges. The 15f capacitor gives a range up to 40 000 electrons which is equivalent to ~200keV and is present in both the 80x80 and 20x20 ASIC. In the 20x20 ASIC low gain can be achieved with the 15f + 135f capacitors, giving an input range of 400 000 electrons which is equivalent to ~2MeV. In the 80x80 ASIC the low gain can be achieved with the 15f + 35f capacitors, giving an input range of 133 000 electrons which is equivalent to ~670keV. The high and low gain modes are selected using a 1 bit digital control input. The ASICs are optimised for the high gain modality.

3.3 Shaper

A band pass filter is used to filter out low and high frequency noise contributions at the output of the preamplifier, and CR-RC type configuration provides a convenient voltage pulse shape for further processing. The shaping time was set to 1.25μs.

3.4 2nd Order Low Pass Filter

A second, low pass filter is required to attenuate the high frequency noise at the output of the CR-RC shaper. The filter is a 2nd order configuration shown in figure 6. Capacitor C1 has been adjusted to give unity gain across the filter. The effect on the pulse peaking time is to increase it from 1.25μs at the output of the CR-RC shaper to 2μs at the output of the low pass filter.

3.5 Peak Hold

The peak amplitude of the filter output needs to be held long enough for it to be sampled prior to read-out. This time will vary depending on when the signal occurs within a read-out frame, and how many pixels have been selected for read-out. This function is performed by the peak hold circuit.

It is possible that a signal can still be rising when the peak hold circuit is sampled and readout. To identify these events the filter output is sampled before and after the peak hold is sampled. The magnitude of the voltage on the filter and the peak hold can be compared by the user off-chip to identify these events. The sampling is conducted by a track and hold circuit.

3.6 Track and Hold

A *track and hold circuit* is used to sample the peak hold and filter outputs. A source follower buffers the held sample onto the column output. The source follower is kept biased by a small trickle current when it is not driving the output bus. A switch then connects the source follower onto the output bus where a larger current source common to all pixels in a column supplies sufficient current to meet speed requirements.

3.7 Control Registers

There are three independent registers which control regions of interest within the pixel array:

- Power Enable Register
- Calibrate Enable Register
- Read Enable Register

The *power enable register* defines the region of pixels which are powered up with the nominal bias current. The Calibrate Enable Register defines the region of pixels which are connected to the calibrate input. The *read enable register* defines the region of pixels that will be read out. These three registers comprise a row and column section. Where the registers are loaded with '1's and intersect, defines the regions of interest. All three registers have independent clocks, but common row and column data inputs. Figure 3 shows regions defined within the pixel array for the 20x20 ASIC. The same process and performance is achieved by the 80x80 ASIC but the registers are 80bits long.

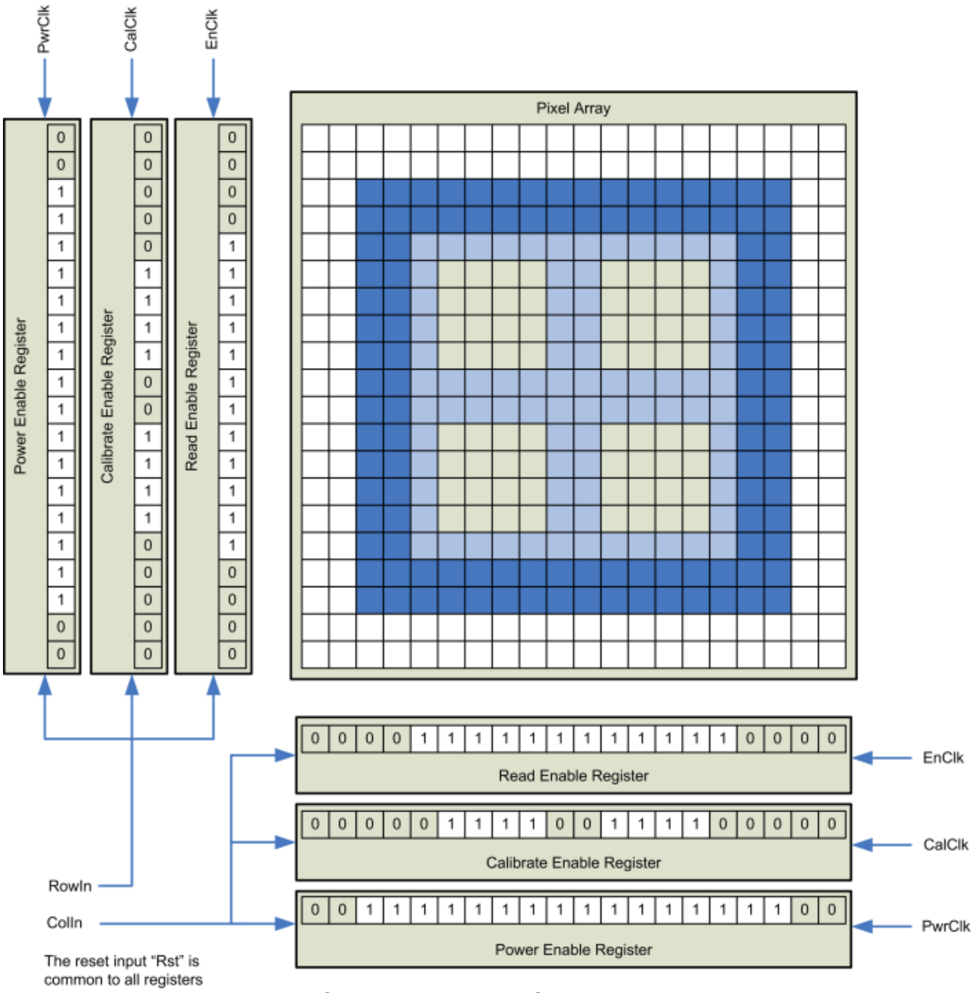

Figure 3. Defining Regions of Interest

3.8 Row Pointer

The *row pointer* is a 20 (20x20) or 80 (80x80) bit shift register with an active skip control allowing those rows not selected for read-out to be ignored. The row pointer is clocked by the signal *RowClk* and requires *m+1* clock pulses for a full readout frame, where *m* is the number of rows enabled for read-out. Five internal signals are generated and output to each pixel in the row to which the *row pointer* is pointing. These occur at the start of a row read-out cycle, and are controlled using pulses on the *Sclk* input (see figure 4). The five signals are:

- S1 - track and hold control for the 1st Filter sample
- SPH - track and hold control for the Peak Hold sample
- S2 - track and hold control for the 2nd Filter sample
- PHRST - Peak Hold reset control
- ENO - control which enables output onto column bus

The width of the peak hold reset pulse PHRST is controlled using the separation of the rising edges of the 2nd and 3rd Sclk pulses.

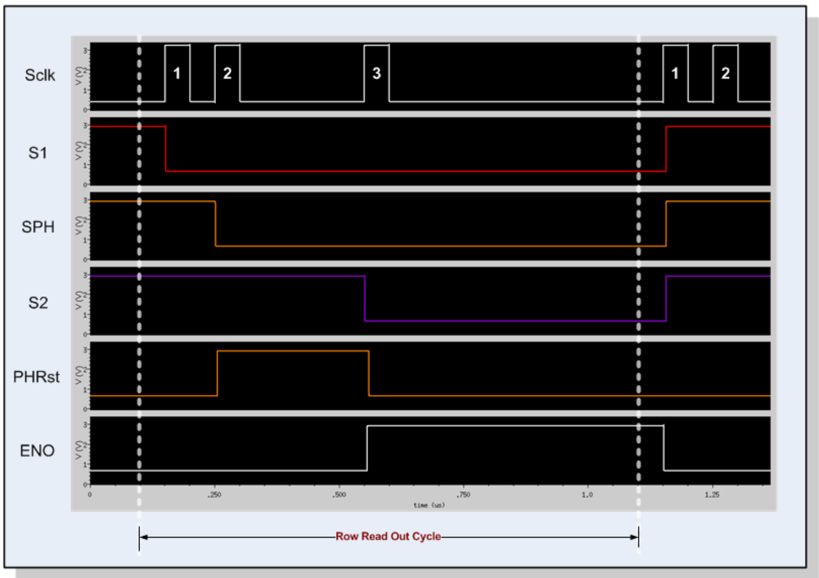

Figure 4. Control Signals Generated from Sclk

3.9 Column Pointer

The *column pointer* selects the columns that have been selected for read-out to be output through the *analogue multiplexer*. Like the *row pointer*, it is a 20 bit shift register in the 20x20 ASIC and there are 4 20bit shift registers in the 80x80 ASIC, all with skip control. The Column Pointer is clocked by the signal *ColClk* and requires *n+1* clock pulse for a full column read-out cycle. This function is described in more detail later in the document. The only outputs from this block are to the *analogue multiplexer*.

3.10 Temperature Diode

The 80x80 ASIC has an a diode that can be connected to the MAXIM MAX6627MKA#T (SOT23 package) chip for a measurement of the temperature of the ASIC.

4. Set-up and running

Following power-up, the HEXITEC ASIC has first to be initialised:

1. Reset ASIC by pulsing *Rst* input high for at least 40ns.
2. Load *Power Enable* Register.
3. Load *Calibrate Enable* Register.
4. Load *Read Enable* Register.
5. Begin frame read-out.

4.1 Loading the Control Registers

Following a reset, all pixels within the array are fully powered up, connected to the calibrate input and enabled for read-out. If this is not the desired case, then the control registers will have to be reprogrammed.

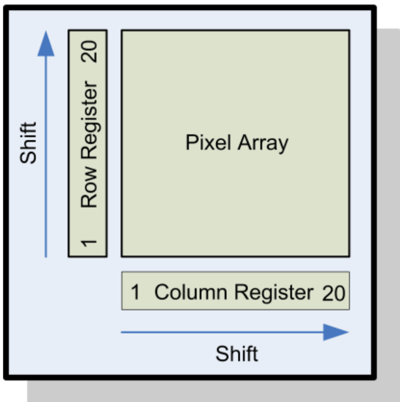

Figure 5. Register Load Direction

The three control registers are each comprised of two 20-bit or 80-bit shift registers as shown in figure 5 for the case of the 20x20 ASIC. One shift register controls columns and the other rows. Data is loaded in at the bottom left corner of the ASIC and shifts upwards (in the case of the row control) and towards the right (in the case of the column control). Data can be loaded into the column and row registers at the same time.

Figure 6 shows the order that the control bits are loaded for the example of the 20x20 ASIC. Bit 20 (or 80) is applied first and shifts to the end of the register after twenty clock cycles. Bit 1 is loaded at the end.

The data is input to the registers using the inputs *Colin* and *RowIn*, which are common to all three registers. The data is clocked in using *EnClk*, *CalClk* and *PwrClk,* which are specific to each register.

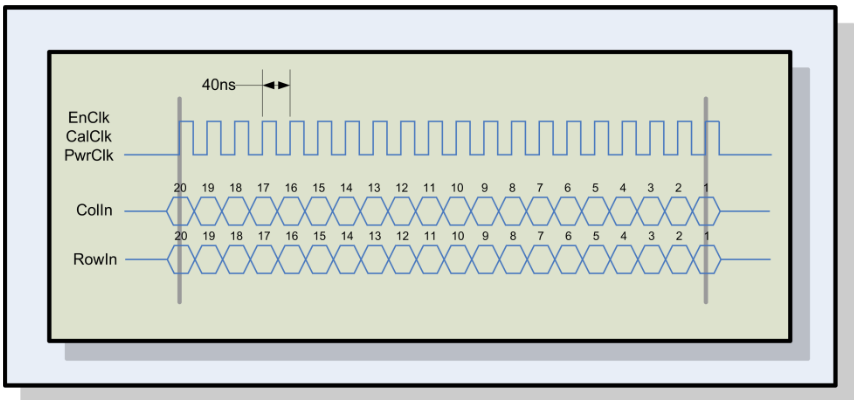

Figure 6. Register Load Sequence

4.2 Pixel Frame Read-out

A full pixel frame readout requires three control signals. Figure 7 shows the operation required to read out one full row of the pixel array. Firstly, the row pointer must be clocked to the row to be read out by pulsing *RowClk*. Secondly the three pulses on *Sclk* are required to sample the signals on the *filter* and *peak hold* outputs. These also generate the *peak hold* reset and output enable signals (see section 3.8). Thirdly, *ColClk* must be pulsed 20 times for the 20x20 and 80x80 ASIC (for the 4 80x20 outputs). Lastly, an extra pulse is required at the end of the row read-out cycle. This clocks the column pointer back to its *parked* position. This cycle can then be repeated as many times as is required to read out all of the rows.

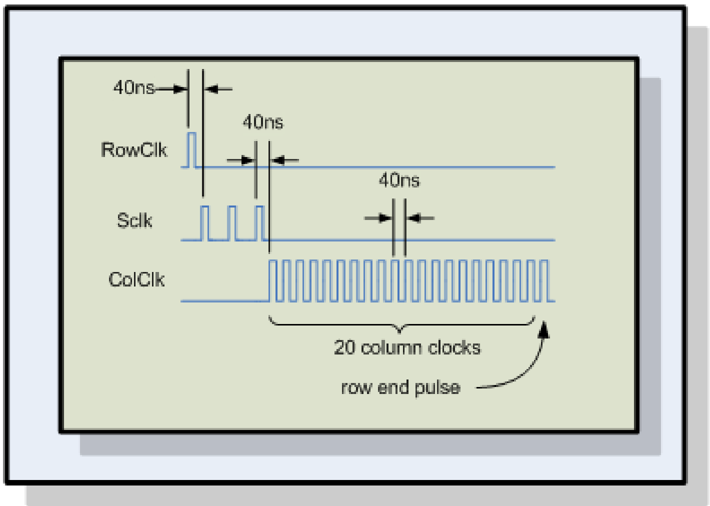

Figure 7. Row Read-out Cycle for 20 Columns

It may be the case that not all of the row or columns are required to be read out. Figure 8 shows a full frame read-out for 5 rows and 5 columns of the pixel array. Prior to the read-out cycle, the *Read Enable Register* has been programmed with the required rows and columns to be read out.

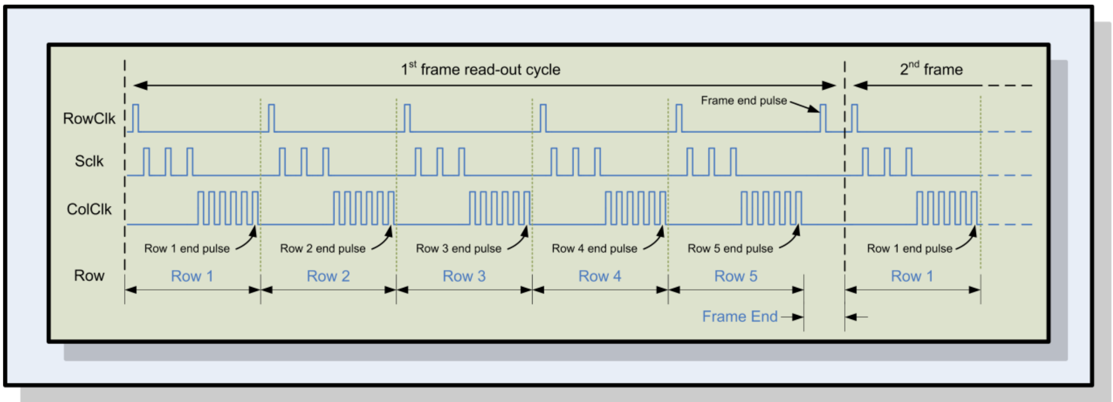

Figure 8. Frame Read-out Cycle for 5 Rows and 5 Columns

The *Row Pointer* waits for the first *RowClk* pulse before moving to the first row that is selected for read-out by the *Read Enable Register,* skipping over all those rows before it. *Sclk* is then pulsed three times to generate the control signals which store the three samples, reset the *peak hold* and enable the column output. Once the three samples are held on the column outputs, *ColClk* is pulsed five times to pass the data from the five enabled columns through the analogue multiplexer to the output. During operation, the *Column Pointer* will skip all columns not selected for read-out by the *Read Enable Register*. A sixth pulse on *ColClk* is required to return the *Column Pointer* to its parked position.

This process is then repeated four more times until the last row has been read out. Following this, one more clock pulse is required on *RowClk* to return the *Row Pointer* to its parked position. The whole process can then be repeated to read out another frame of data.

This example is for five column and five row read-out. Note that *m column* and *n row* read-out requires *m+1* pulses on *ColClk* and *n+1* pulse on *RowClk*.

5. Data Format

Output data is synchronised with the rising edge of the *ColClk.* The minimum separation of *ColClk* pulses should be 40ns. The dynamic output range is 1V but due to process variations the signal can lie in the range 0.2V to 1.9V (see figure 9).

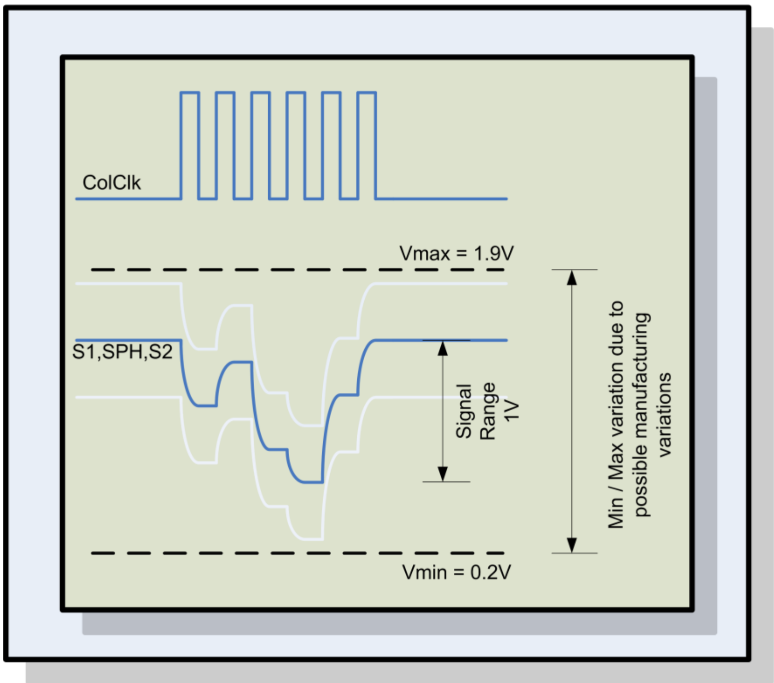

Figure 9. Output Data Format

6. Pad List and Position

A picture of the pad position on the chip is shown in figure. 10

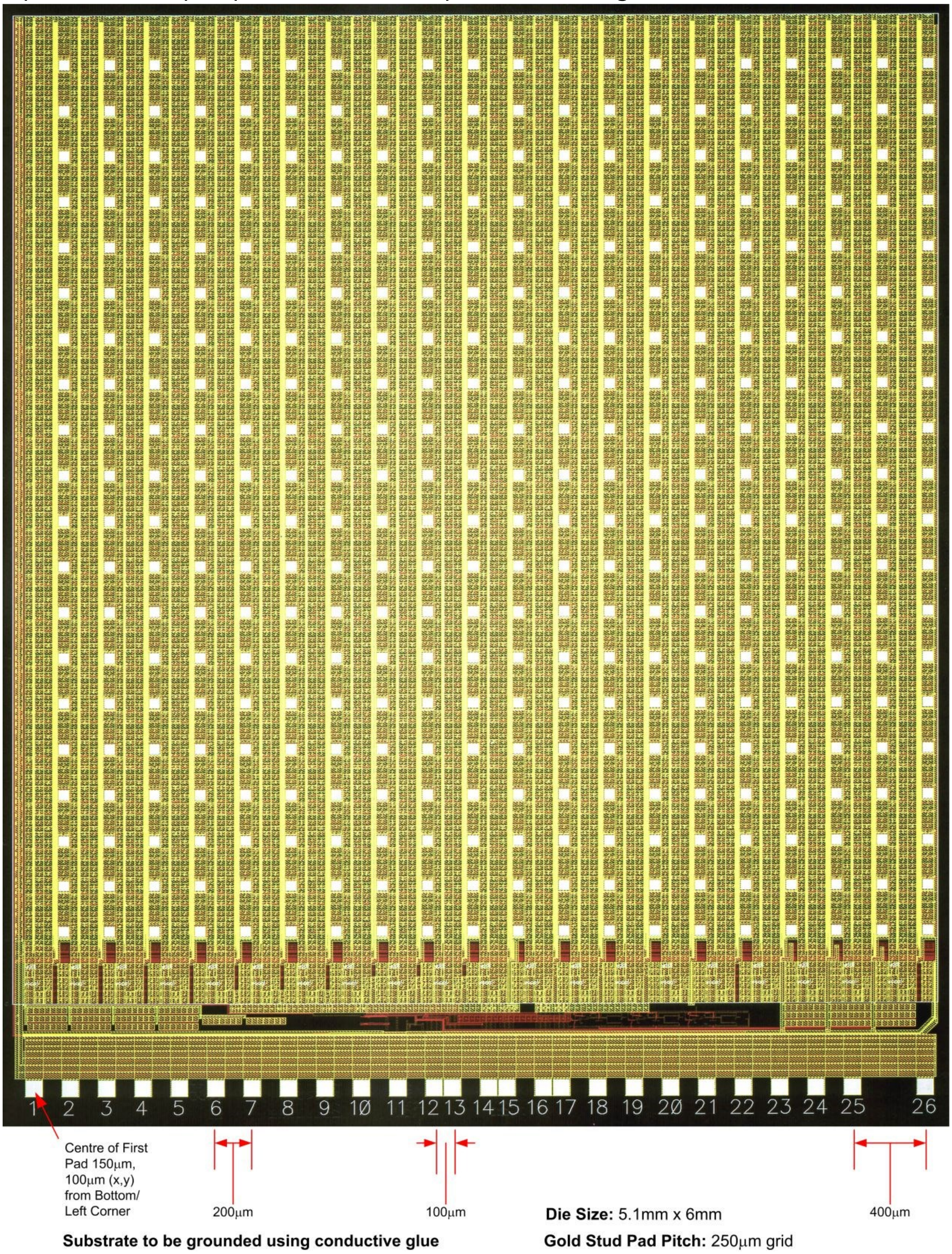

Figure 10. I/O Pad Positions

Table 1. HEXITEC 20x20 I/O List

Pad No.	Name	Type	Function
1	GNDD	supply	digital ground (0V)
2	VDDD	supply	digital power (3.3V)
3	Sclk	CMOS input	sample clock
4	RowClk	CMOS input	row clock
5	ColClk	CMOS input	column clock
6	PwrClk	CMOS input	power enable register clock
7	EnClk	CMOS input	readout enable register clock
8	CalClk	CMOS input	calibration enable register clock
9	ColIn	CMOS input	enable registers input (columns)
10	RowIn	CMOS input	enable registers input (rows)
11	Rst	CMOS input	register reset
12	GNDA	supply	analogue ground (0V)
13	GNDA	supply	analogue ground (0V)
14	VCCA	supply	preamp supply voltage (1.65V)
15	VCCA	supply	preamp supply voltage (1.65V)
16	VDDA	supply	analogue power (3.3V)
17	VDDA	supply	analogue power (3.3V)
18	S1	analogue output	first shaper sample
19	SPH	analogue output	peak hold sample
20	S2	analogue output	second shaper sample
21	Gain	digital input	preamplifier gain select
22	Ibias	current input	input bias current (80uA)
23	VN	analogue output	decoupling point
24	VC	analogue output	decoupling point
25	VP	analogue output	decoupling point
26	VCAL	analogue input	Calibration voltage input

Table 2. Decoupling for 20x20

Pin	Name	Capacitance
2	VDDD	100nF to Ground
14	VCCA	100nF to Ground
16	VDDA	100nF to Ground
22	Ibias	100nF to Ground
23	VN	100nF to Ground
24	VC	100nF to Ground
25	VP	100nF to Ground

Table 3. HEXITEC 80x80 I/O List
Note that not all power and decoupling must be connected to for the ASIC to operate.

Pad No.	Pad Offset (μm)	Name	Type
0	0	DET_1	Connection to pad for guard band or steering gird connection.
1	195	GNDD	Supply (0V)
2	390	VDDD	Supply (3.3V)
3	585	Sclk	CMOS input
4	780	RowClk	CMOS input
5	975	GNDA	supply
6	1170	PwrClk	CMOS input
7	1365	EnClk	CMOS input
8	1560	CalClk	CMOS input
9	1755	ColIn	CMOS input
10	1950	RowIn	CMOS input
11	2145	Rst	CMOS input
12	2340	GNDA	Supply (0V)
13	2490	GNDA	Supply
14	2685	VCCA	Supply (1.65V)
15	2835	VCCA	Supply
16	3030	VDDA	Supply (3.3V)
17	3180	VDDA	supply
18	3375	S1_1	analogue output
19	3570	SPH_1	analogue output
20	3765	S2_1	analogue output
21	3960	Gain	digital input
22	4155	Ibias	current input - bias of 320uA (2.5kΩ to Vdd)
23	4350	VN_1	analogue output
24	4545	VC_1	analogue output
25	4740	VP_1	analogue output
26	5000	DET_2	Connection to pad for guard band or steering gird connection.
27	5195	GNDA	
28	5390	GNDA	
29	5585	VCCA	
30	5780	VCCA	
31	5975	VDDA	
32	6170	GNDA	
33	6385	GNDA	
34	6560	VCCA	
35	6755	VCCA	
36	6950	VDDA	
37	7145	VDDA	
38	7340	GNDA	
39	7490	GNDA	
40	7685	VCCA	
41	7835	VCCA	
42	8030	VDDA	

43	8180	VDDA	
44	8375	S1_2	analogue output
45	8570	SPH_2	analogue output
46	8765	S2_2	analogue output
47	8960	GNDA	
48	9155	VCCA	
49	9350	VN_2	analogue output
50	9545	VC_2	analogue output
51	9740	VP_2	analogue output
52	10000	DET_3	Connection to pad for guard band or steering gird connection.
53	10195	GNDA	
54	10390	GNDA	
55	10585	VCCA	
56	10780	VCCA	
57	10975	VDDA	
58	11170	GNDA	
59	11365	GNDA	
60	11560	VCCA	
61	11755	VCCA	
62	11950	VDDA	
63	12145	VDDA	
64	12340	GNDA	
65	12490	GNDA	
66	12685	VCCA	
67	12835	VCCA	
68	13030	VDDA	
69	13180	VDDA	
70	13375	S1_3	analogue output
71	13570	SPH_3	analogue output
72	13765	S2 _3	analogue output
73	13960	GNDA	
74	14155	VCCA	
75	14350	VN_3	analogue output
76	14545	VC_3	analogue output
77	14740	VP_3	analogue output
78	15000	DET_4	Connection to pad for guard band or steering gird connection.
79	15195	GNDA	
80	15390	GNDA	
81	15585	VCCA	
82	15780	VCCA	
83	15975	ColClk	CMOS input
84	16170	GNDA	
85	16365	GNDA	
86	16560	VCCA	
87	16755	VCCA	
88	16950	VDDA	
89	17145	VDDA	
90	17340	GNDA	

91	17490	GNDA	
92	17685	VCCA	
93	17835	VCCA	
94	18030	VDDA	
95	18180	VDDA	
96	18375	S1_4	analogue output
97	18570	SPH_4	analogue output
98	18765	S2_4	analogue output
99	18960	diodeP	current input – Temperature Diode
100	19155	diodeN	current output– Temperature Diode
101	19350	VN_4	analogue output
102	19545	VC_4	analogue output
103	19740	VP_4	analogue output
104	19935	VCAL	analogue input

Table 4. Decoupling for 80x80

Pin	Name	Capacitance
2	VDDD	100nF to round
14,15,29,30,34, 35,40,41,48,55, 60,61,66,67,74, 81,82,92,93	VCCA	100nF to round
16,17,31,36,37, 42,43,57,62,63, 88,89,94,95	VDDA	100nF to round
22	Ibias	100nF to round
23,49,75,100	VN *x*	100nF to round
24,50,76,101	VC *x*	100nF to round
25,51,77,102	VP *x*	100nF to round

7. Readout Schematic

A suggested schematic for operating the HEXITEC 20x20 ASIC is shown in figure 11. The same bias current, bias and power supply decoupling should be applied to the HEXITEC 80x80 ASIC. Not all decoupling and power supplies must be made to the 80x80 ASIC, it has been shown to work with only the same power supply and bias decoupling as the 20x20 ASIC. The analogue power supplies must be low noise for the best spectral performance. The 80x80 ASIC will have the same analogue outputs to the DAQ repeated 4 times.

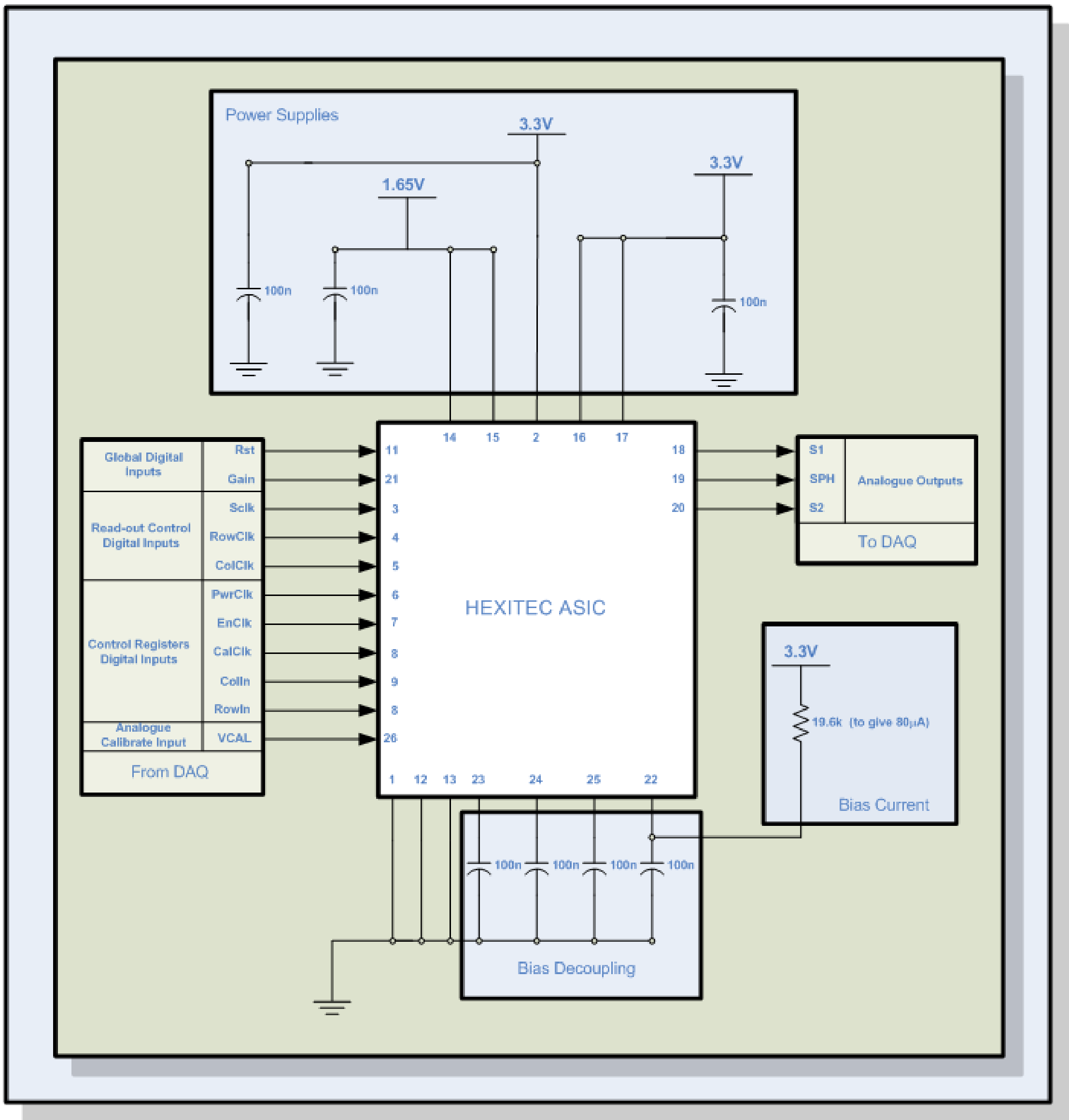

Figure 11. Read-out Schematic for the HEXITEC 20x20 ASIC

8. Test Pulse

A test or “calibration” circuit is included for characterising the pixel electronics. A step voltage applied to the calibration input *VCAL* will inject a charge through the calibration capacitor within each pixel selected by the *calibrate enable register*. The charge injected must have the correct polarity and a falling edge is necessary on *VCAL* to achieve this. The amount of charge is dependent on the step height which should be in the range 0V to 3V. In high gain a pulse going from 0.2-0V will generate an output at roughly two thirds of the output range (~0.6V).

A calibrate sequence is synchronised to every three frames of read-out (figure 12). The calibrate input *VCAL* starts at GND (0V) and at the start of the first frame (i.e. on the rising edge of the first *colclk*) *VCAL* rises to the calibration voltage *Vcal* (in the range 0-3V). It then remains at this voltage during the whole of the *Frame 1* read-out cycle. *VCAL* then returns to GND at the start of *Frame 2* or anywhere between the start of *Frame2* to the end of *Frame3* (last *colclk*). A new calibration sequence starts at the beginning of *Frame 4* at which time*VCAL* returns to the calibration voltage *Vcal*.

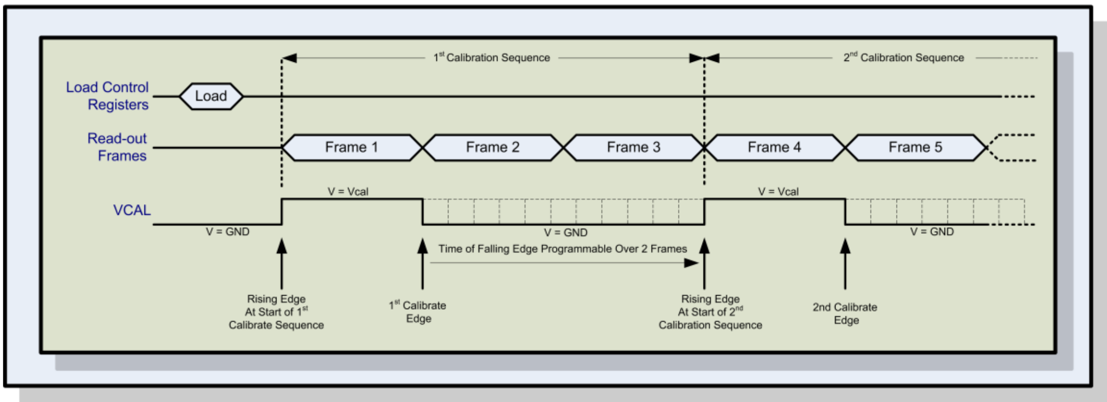

Figure 12. Calibration Sequence

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