RCloud Tasking Form – Part B: Statement of Requirement (SoR)

Title of Requirement	**Quantum Error Correction Design Study**
Requisition No.	RQ0000024072
SoR Version	**0.1**

1.	**Statement of Requirements**
1.1	**Summary and Background Information**
	MOD DST, with NSSIF, are procuring quantum photonic processing systems from the UK SME ORCA Computing Ltd. ORCA is the only manufacturer anywhere in the world of low SWaPC quantum photonic computing systems which can solve militarily important problems in optimisation and machine learning; later versions of the technology, expected in 5 – 10 year's time, will be universally programmable and (in principle) will be able to solve any problems. Through the "AI and Autonomy in the ISR Enterprise" (A2ISR) project, Dstl is working closely with ORCA to understand and assess for military use the unique photonic quantum processing systems which in their current form are potentially field deployable. Several military use cases have already been identified and more are possible if the problems can be solved which arise from loss of quantum information encoded in the photons manipulated by the ORCA processor; this process is called error correction. The unique features of the ORCA processors include their construction using "components off the shelf" (COTS) and the lack of bulky and power hungry dilution refrigerators. Both factors result in low SWaPC, high VfM, rack mounted systems which could be widely deployed e.g. at the command vehicle level. This obviates the need for the secure, resilient communications necessary to use other types of quantum processor (such as quantum annealers or quantum circuit model processors) and allows quantum solutions to be deployed into the field. The ORCA PT-1 implements time-bin boson sampling, which is a non-universal method of quantum computation with few applications. Despite non-universality, the PT-1 can be used as a variational quantum eigensolver (VQE) to solve machine learning and optimisation tasks (solution of Ising or QUBO problems which are NP hard) and Boson sampling is an important milestone on the route to a universal, fault-tolerant photonic quantum computer. The demonstration of a compatible error

correction scheme would be a major step forward in the evolution of the ORCA processor towards universal programmability.

Dstl has worked closely with OxbrdgRbtx, a UK SME, on previous quantum processing studies. OxbrdgRbtx has extensive experience in photonic quantum processing and has generated unique IP which, potentially, could be integrated into, or implemented by, ORCA systems. The result would be a piece of hardware able to demonstrate the error correction code and assess the error flows and trajectories. Together with ancillary photons, it would also be a universal quantum computer which (if the errors scale as expected with system size) will be scalable. The bi-prime number 15 (a number expressible with 4 bits) requires 28 logical qubits for factorisation using Shor's algorithm and this should be achievable by about 2025. Subsequently, computing power could grow rapidly with focused investment following. Published estimates of the required number of real qubits to represent logical qubits vary, but can be as high as several hundred.

This SoR addresses the generation of prototype engineering designs for photonic error correction which will validate the error correction codes and the assumptions underlying them.

The Error Correction Algorithm Problem:

There are many competing technologies in the field of Quantum Information Processing (QIP). In particular, in circuit model Quantum Computation (QC) there are at least half a dozen, very well funded companies. Most of these are photonics based and many have made many claims as to the superiority of their particular approach.

Each has their own variation of hardware and error correction algorithms implemented in that hardware. All of the literature that describes the necessary fidelities or failure probabilities of the steps implemented in this hardware, assumes uncorrelated errors so single gate measurements can be extrapolated to full implementations of solutions.

At the same time, all of these startups are claiming exclusive optimality, but cannot share or show results yet. Some have stated no meaningful results will be released until several more years of work, and funding, have passed.

OxBrdgRbtx has worked to provide a way of evaluating all of the proposed error correction schemes with off-the shelf hardware design.

The Solution:

This study has led to a draft design of a bench top device that can measure the errors of gates in combination and therefore calculate the correlated errors, not only over pairs of contiguous components, but over many complicated designs. The proposed device is reconfigurable so that all of the different algorithms and technologies can be assessed.

	This work will create diagrams, drawings, equations and explanations so that someone with good knowledge in this arena would be able to build the physical device. Future Collaboration: Once the drawings are completed the device would need to be built. There are several possibilities for this, but to keep all the IP in the UK, Dstl may engage further with OxbrdgRbtx and ORCA Computing Ltd whose technology is compatible with the designs produced in this work.
1.2	**Requirement**
	During a project of duration 1 month the project is required to: 1. Generate prototype patchboard photonic circuit design to implement any error correction codes on photonic quantum processing hardware. 2. Show how this prototype patchboard photonic circuit design could be implemented on a chip with suitable switching replacing the patch connectors. 3. Show how a quantum memory could be used to extend the utility of the device to a full quantum computer of polynomial speed. 4. Show how quantum state distribution systems could be used as the above quantum memory.
1.3	**Options or follow on work** 5. Numerical calculations of pairs of components to show how the correlated errors would be calculated from the measurements (Option) If the Design Study is successful, to facilitate building and testing breadboard prototypes compatible with ORCA's proprietary systems OxbrdgRbtx should agree a Non Disclosure Agreement (NDA) with ORCA (and Dstl if necessary), which will facilitate follow on work from this project and enable future collaborative working to build demonstrator error correction systems. Written as requirements these become: 6. Propose in outline, with ROM costs, a follow on simulation project to complement the physical device. 7. Propose in outline, with ROM costs, a follow on project, jointly with ORCA Computing Ltd to build and test photonic error correction circuits.
	Not Applicable
1.4	**Contract Management Activities**
1.5	**Health & Safety, Environmental, Social, Ethical, Regulatory or Legislative aspects of the requirement**

	This will be office based work and a simple IT DSE Assessment only needed

1.6	Deliverables & Intellectual Property Rights (IPR)					
Ref.	**Title**	**Due by**	**Format**	**Expected classification (subject to change)**	**What information is required in the deliverable**	**IPR Condition**
D - 1	Kick-off meeting	Within 2 weeks of contract start	Presentation (pptx or pdf)	[Redacted]	Presentation to include: • Proposed technical approach • Risks (if any) and risk management plan Review of deliverables	DEFCON 705
D - 2	Progress reports	weekly	Meeting notes as a short email	[Redacted]	Short progress meetings conducted by telephone or Teams/Zoom as appropriate	DEFCON 705
D - 3	Final report	T0 + 4 months	Word, PowerPoint or PDF	[Redacted]	The report must capture the technical approach, give prototype designs and details of the proposed follow-on numerical simulation techniques	DEFCON 705

1.7	Deliverable Acceptance Criteria
	as per Framework T&C's

2	Evaluation Criteria
2.1	Method Explanation

	Commercial Assistance needed here before or after a requisition is raised. Framework evaluation criteria as per T&C's may apply.
2.2	Technical Evaluation Criteria
	Commercial Assistance needed here before or after a requisition is raised. Framework evaluation criteria as per T&C's may apply.
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